FIG.1

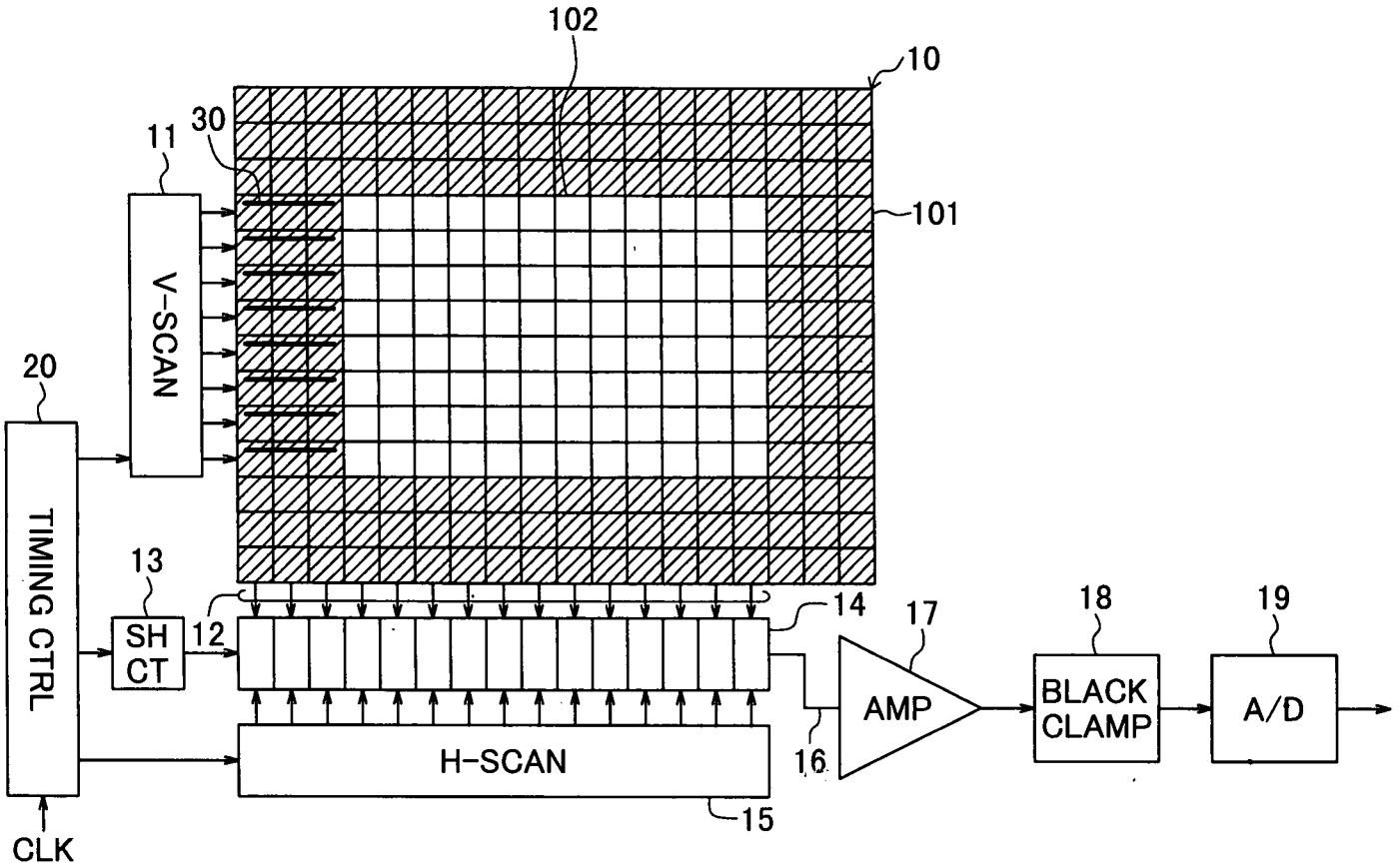

FIG.2

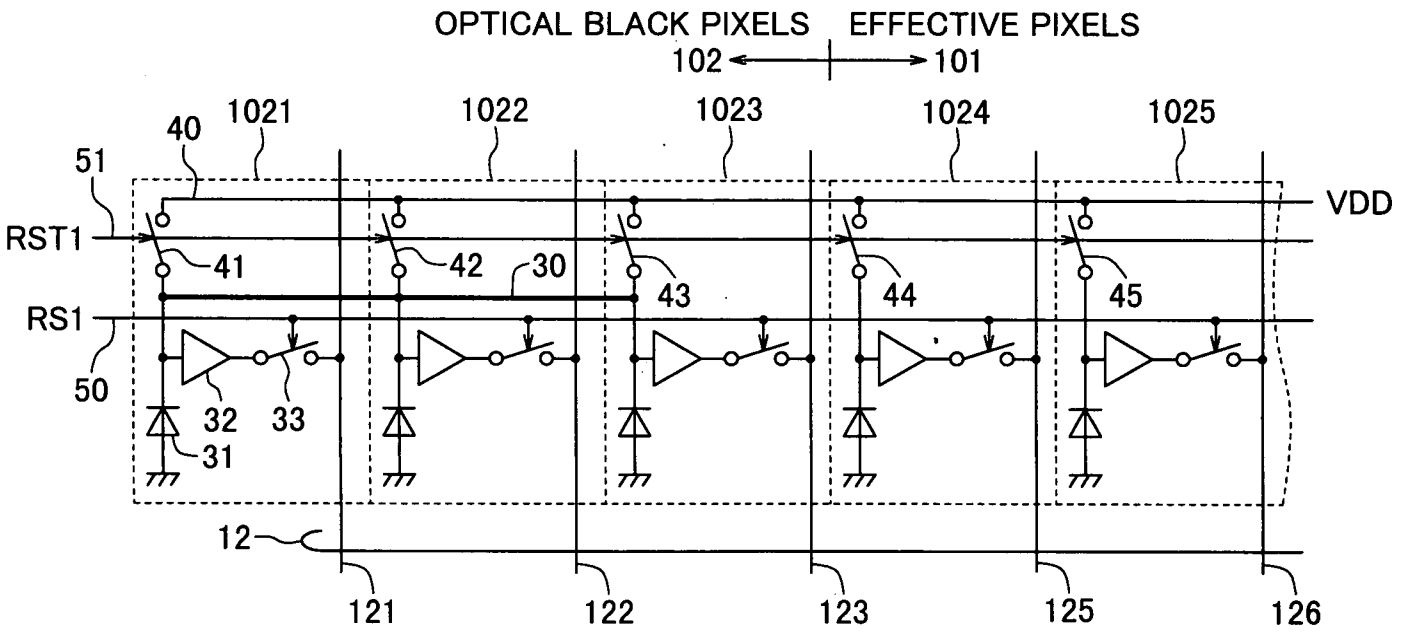

FIG.3

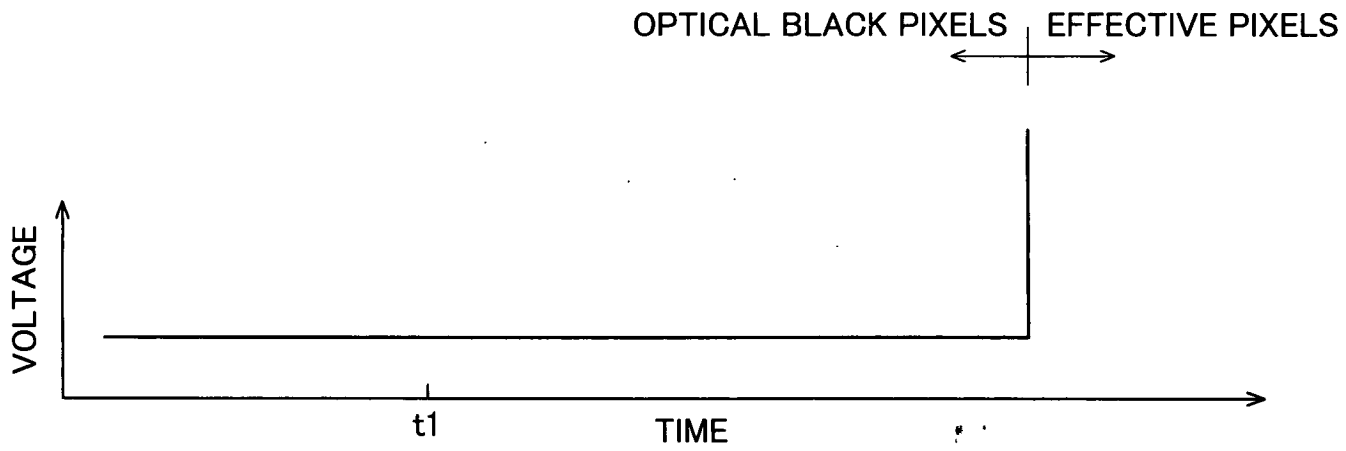

FIG.4

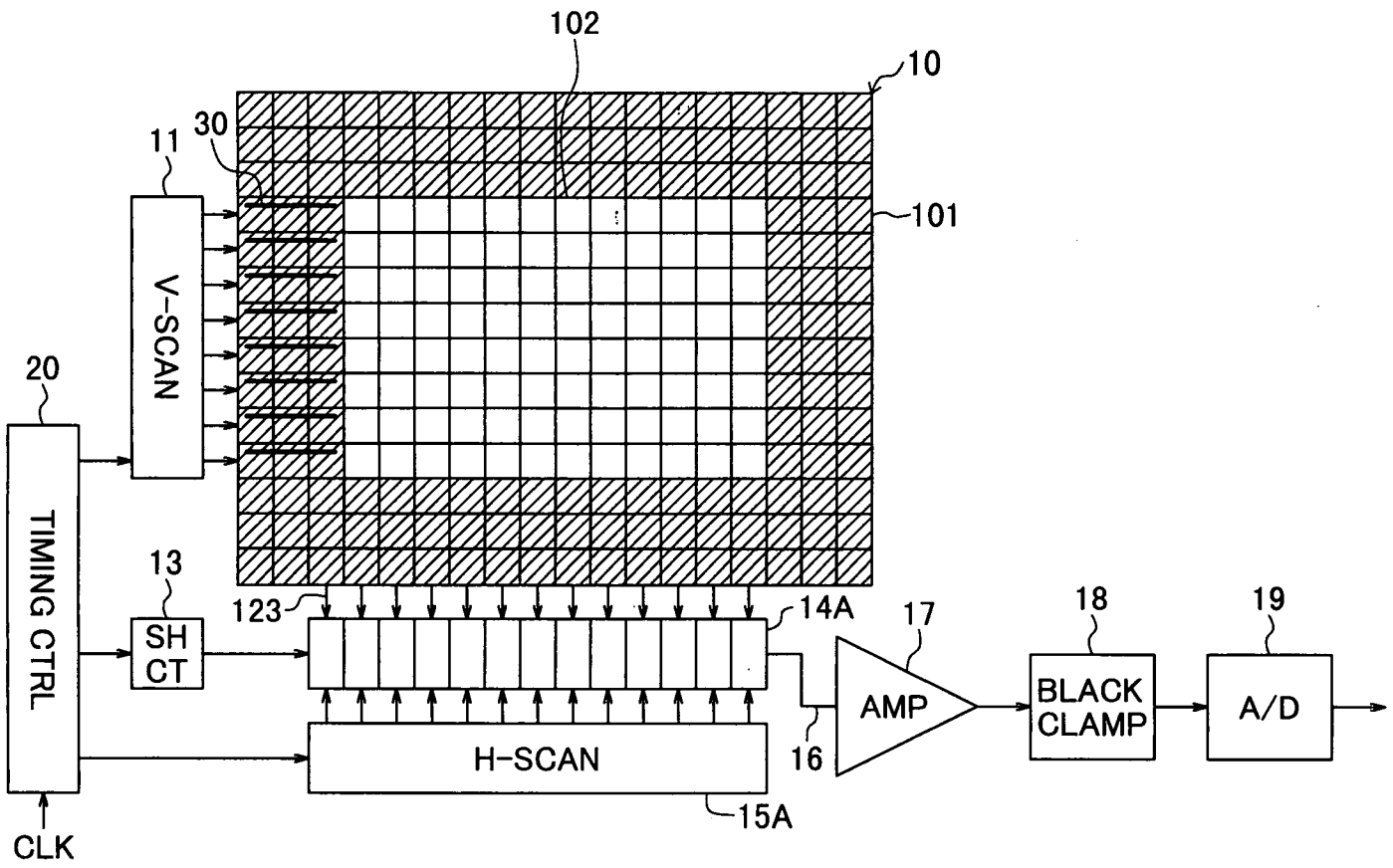

FIG.5

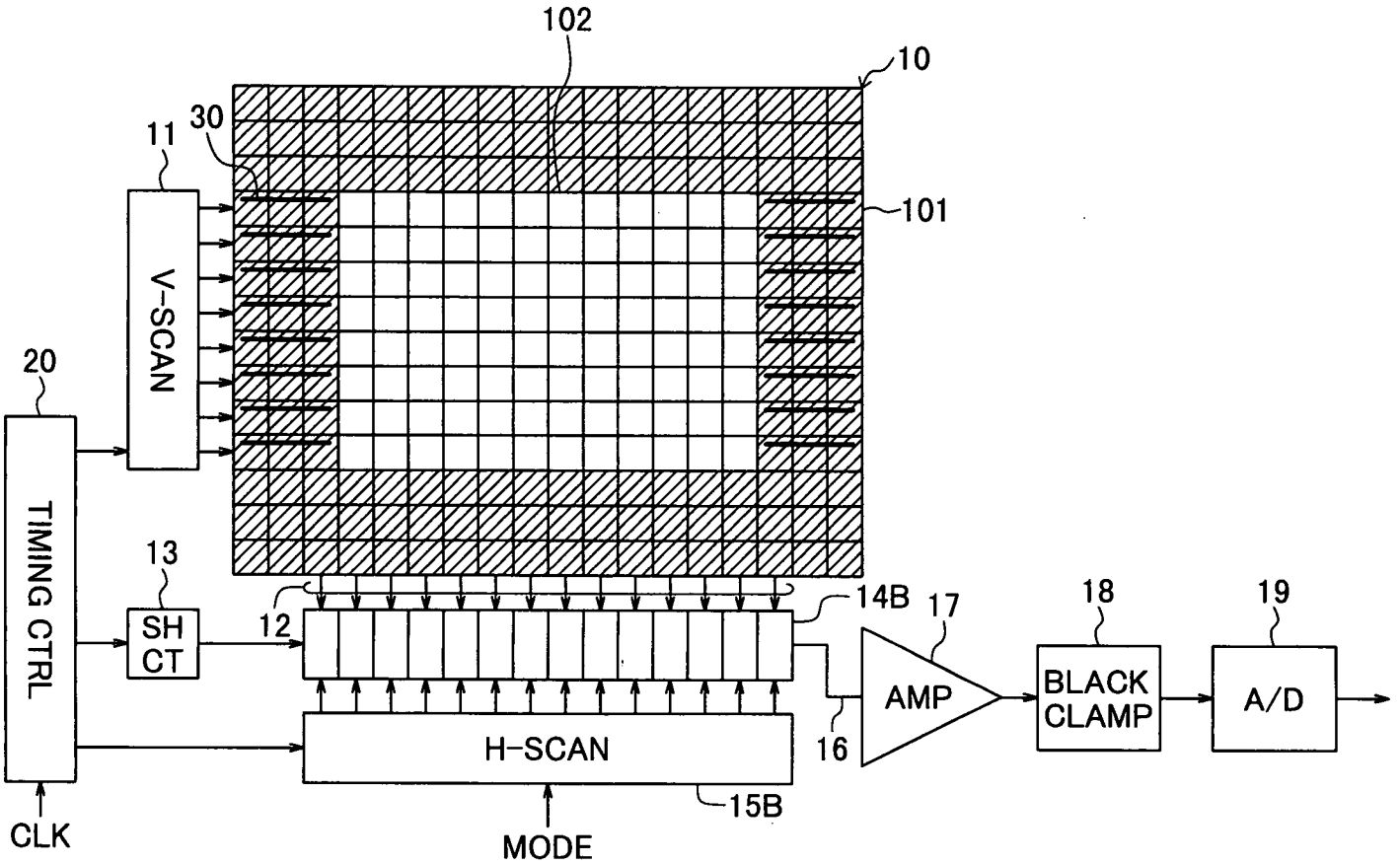
102
10
11
30
101
V-SCAN
20
TIMING CTRL
13
SH
CT
12
14B
17
18
19
AMP
BLACK
CLAMP
A/D
H-SCAN
16
15B
CLK
MODE

FIG.6

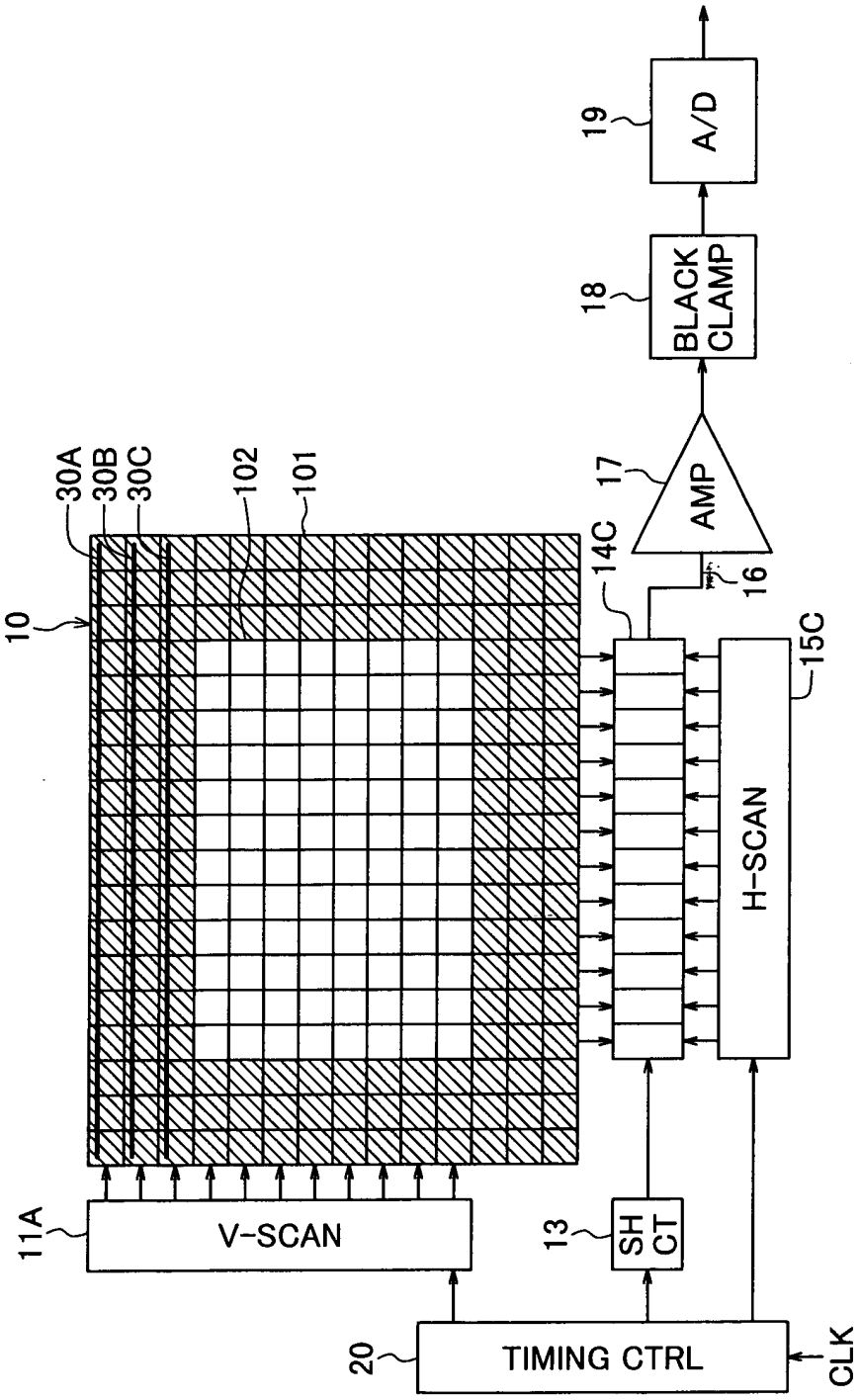
19
A/D
18
BLACK CLAMP
17
AMP
16
14C
15C
H-SCAN
30A
30B
30C
102
101
10
11A
V-SCAN
13
SH CT
20
TIMING CTRL
CLK

FIG.7

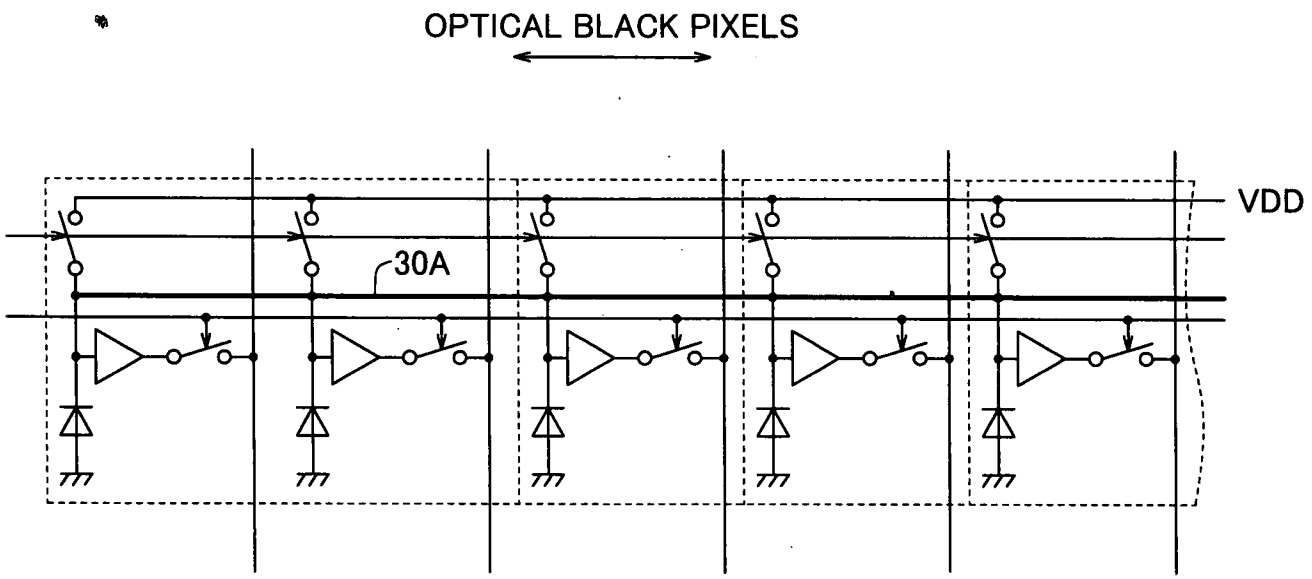

FIG.8

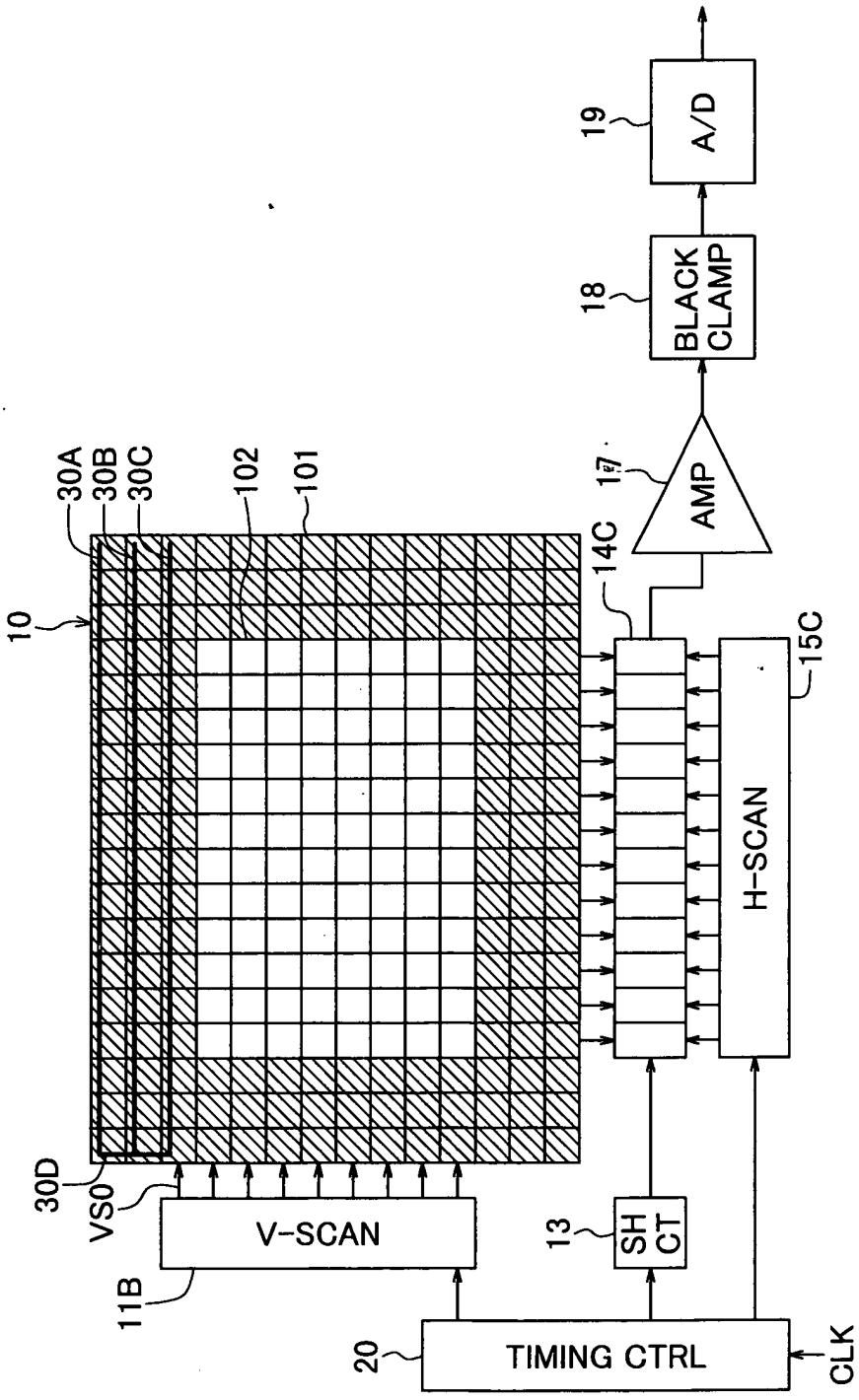
10
30A
30B
30C
102
101
30D
VS0
11B
V-SCAN
13
SH CT
20
TIMING CTRL
CLK
14C
15C
H-SCAN
17
AMP
18
BLACK CLAMP
19
A/D

FIG.9

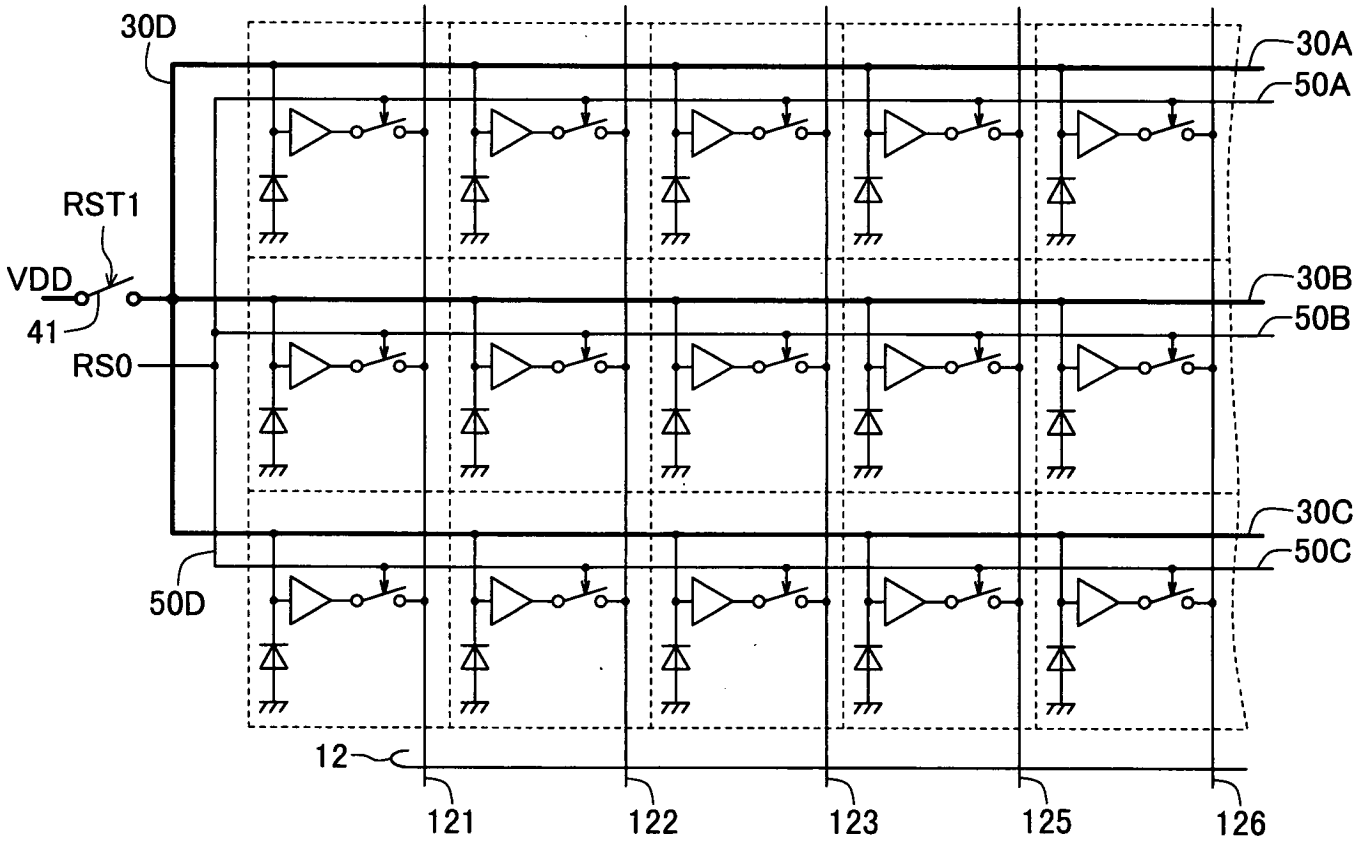

FIG.10

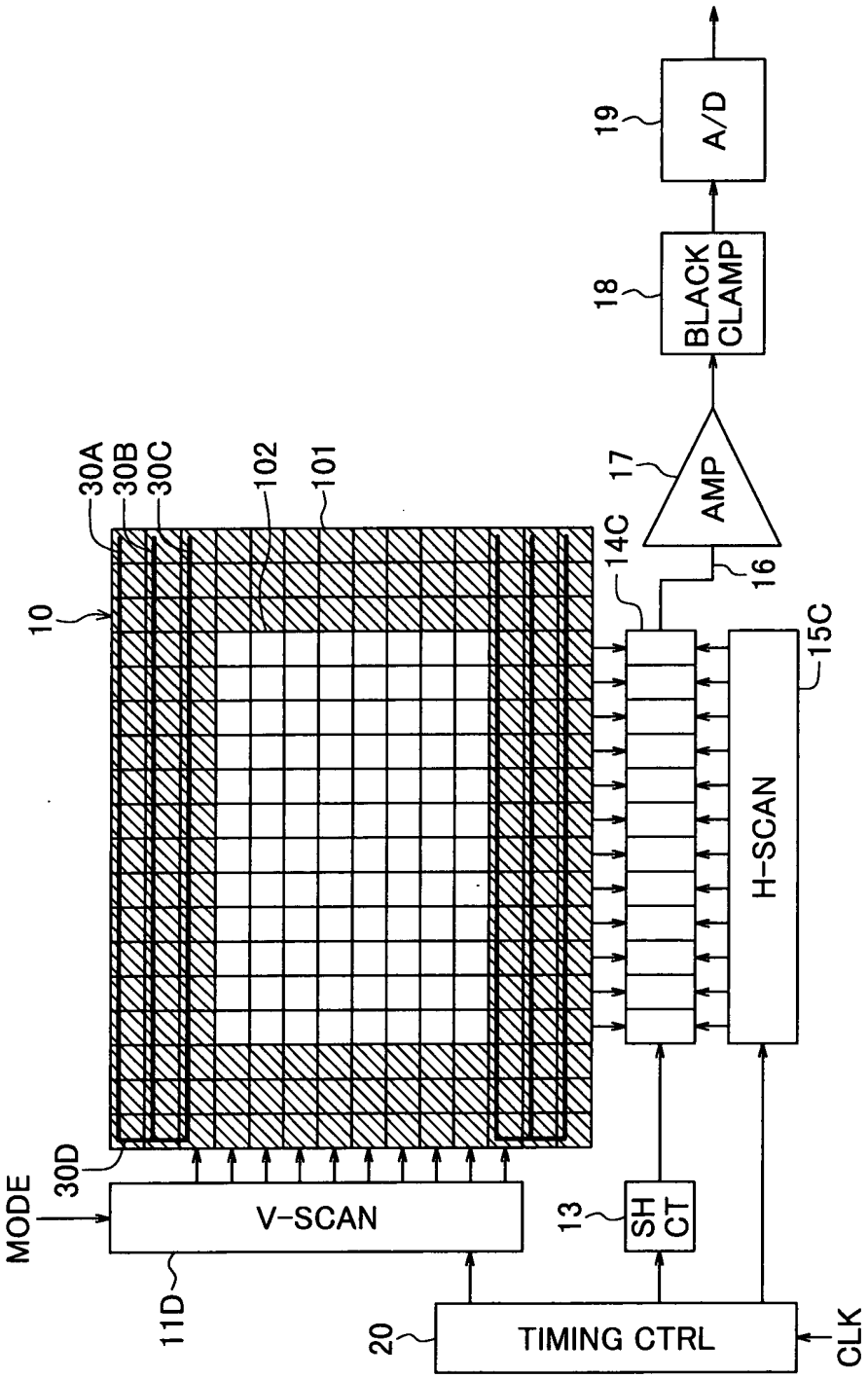
19
A/D
18
BLACK CLAMP
17
AMP
16
14C
15C
H-SCAN
30A
30B
30C
102
101
10
30D
MODE
V-SCAN
11D
13
SH CT
20
TIMING CTRL
CLK

FIG.11

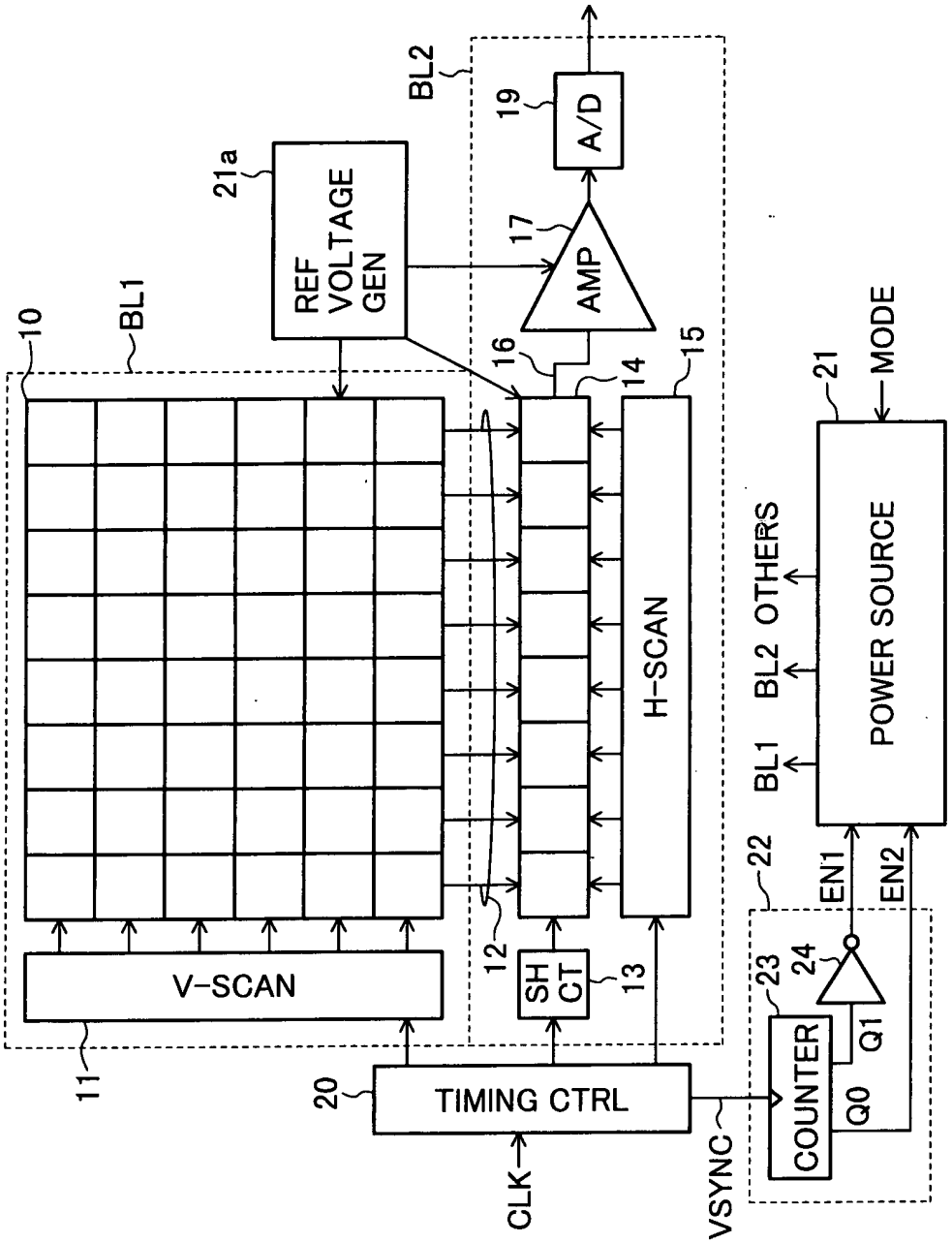
10
BL1
BL2
21a
REF VOLTAGE GEN
19
A/D
17
AMP
16
14
15
H-SCAN
V-SCAN
12
SH CT
13
11
20
TIMING CTRL
CLK
VSYNC
21
MODE
POWER SOURCE
BL1
BL2
OTHERS
22
EN1
EN2
23
24
Q1
Q0
COUNTER

FIG.12

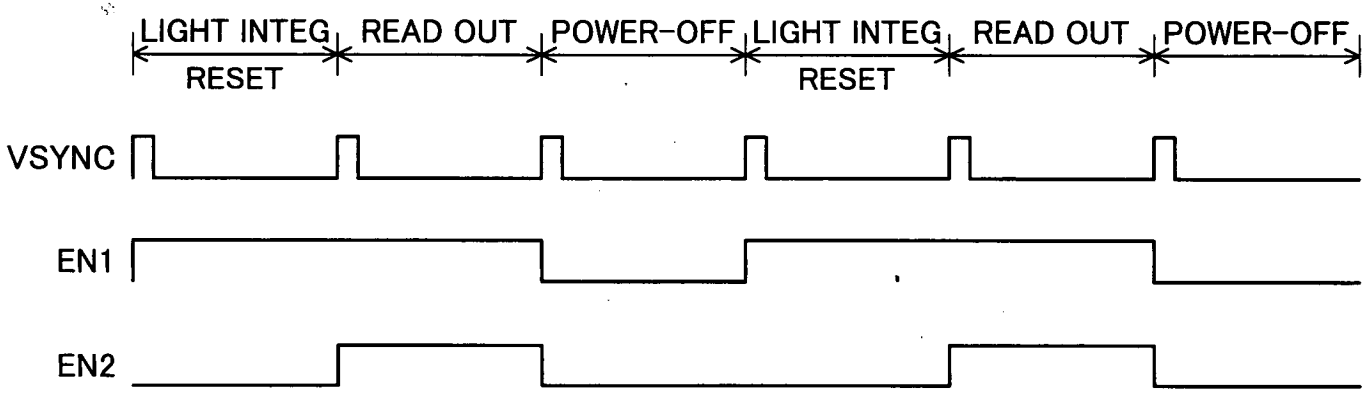

FIG.13

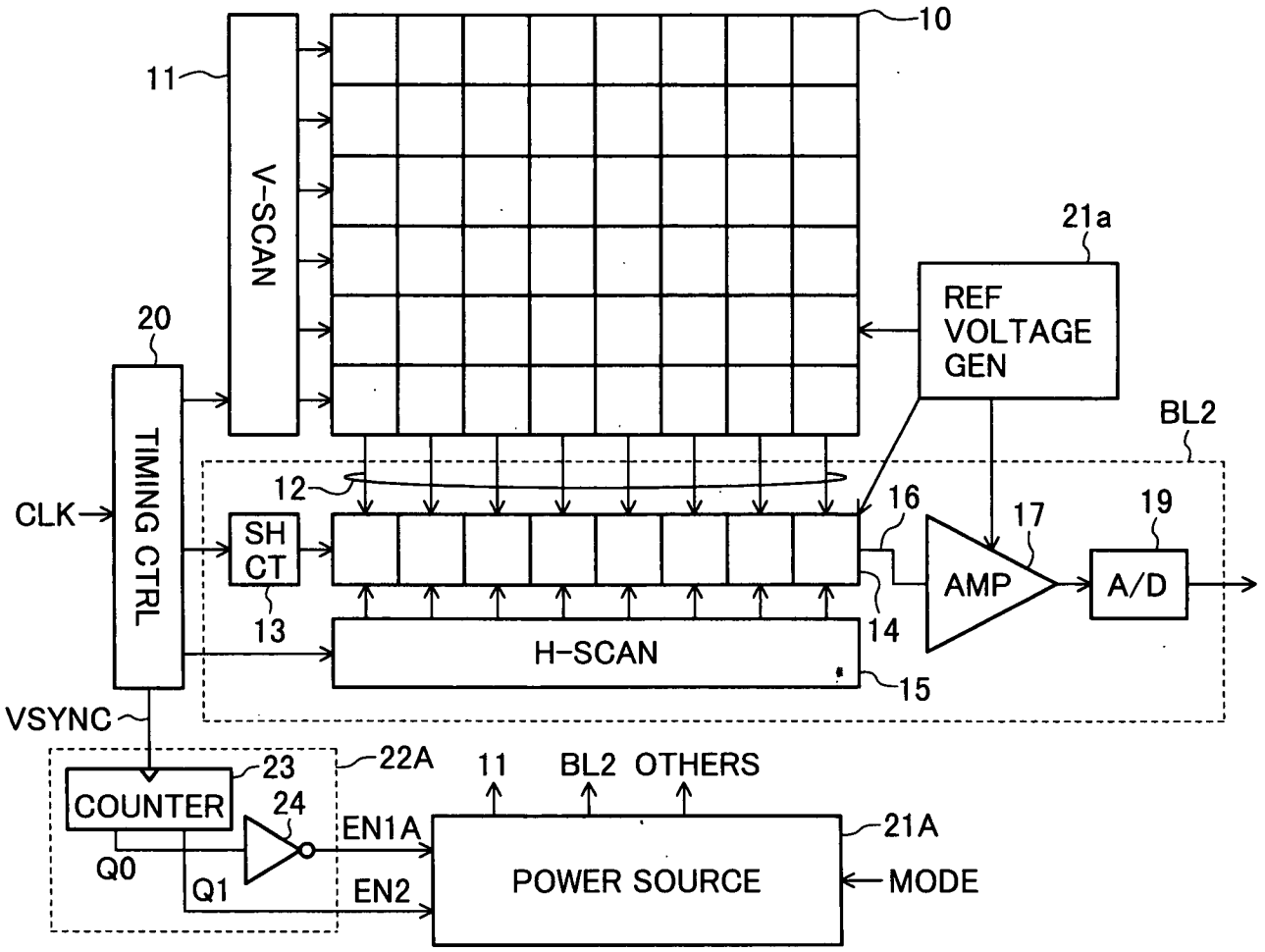

FIG.14

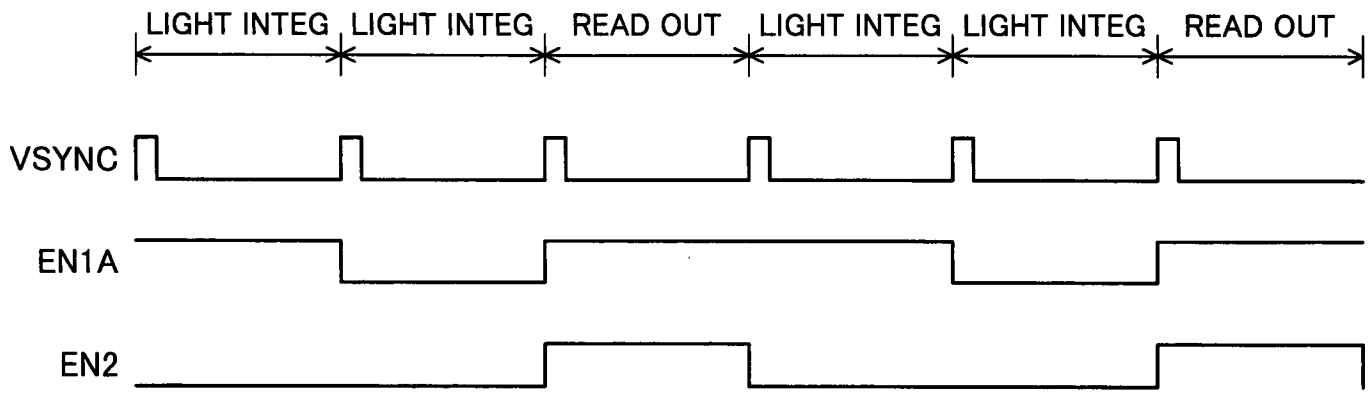
LIGHT INTEG
LIGHT INTEG
READ OUT
LIGHT INTEG
LIGHT INTEG
READ OUT
VSYNC
EN1A
EN2

FIG.15

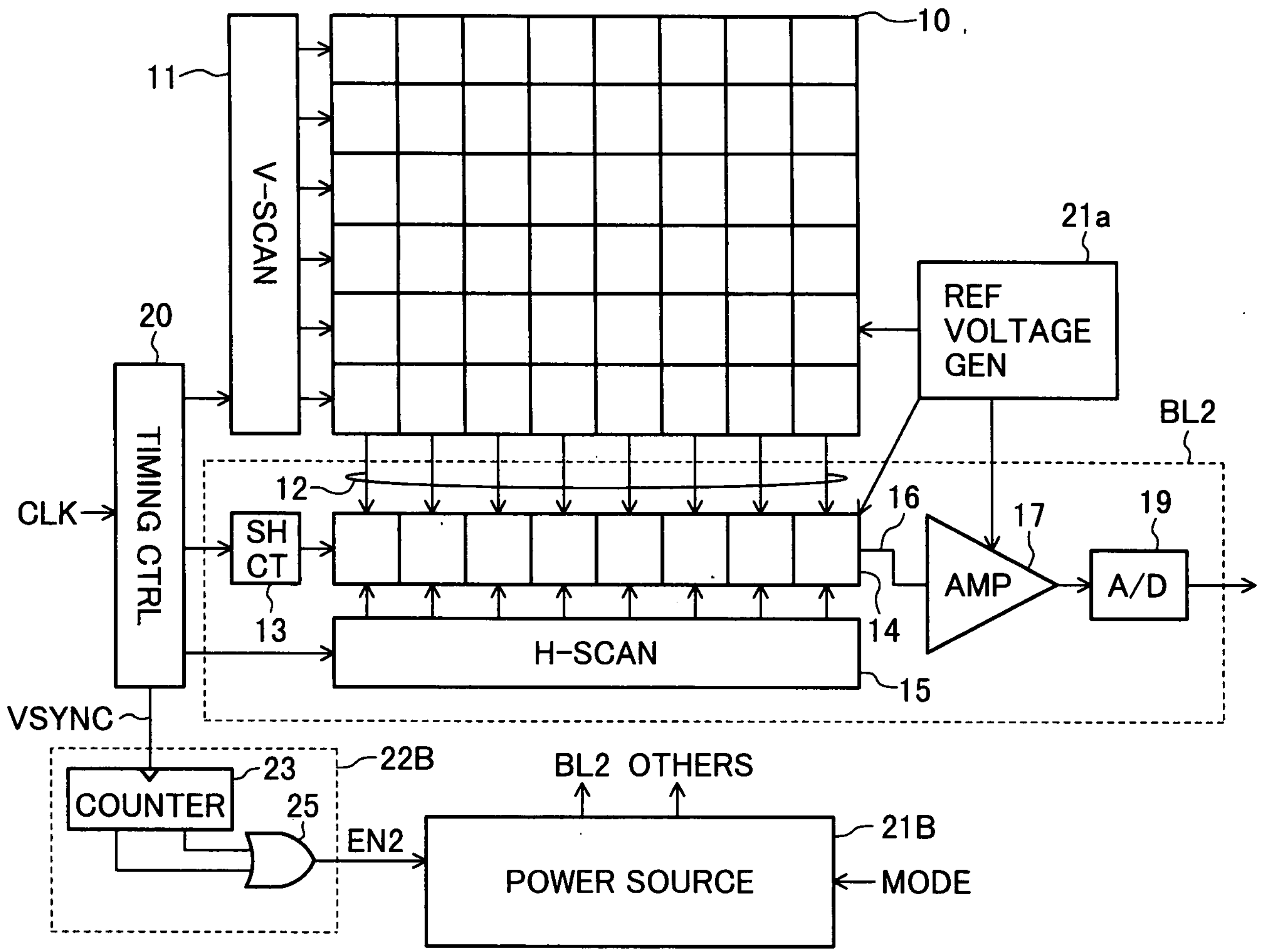

FIG.16

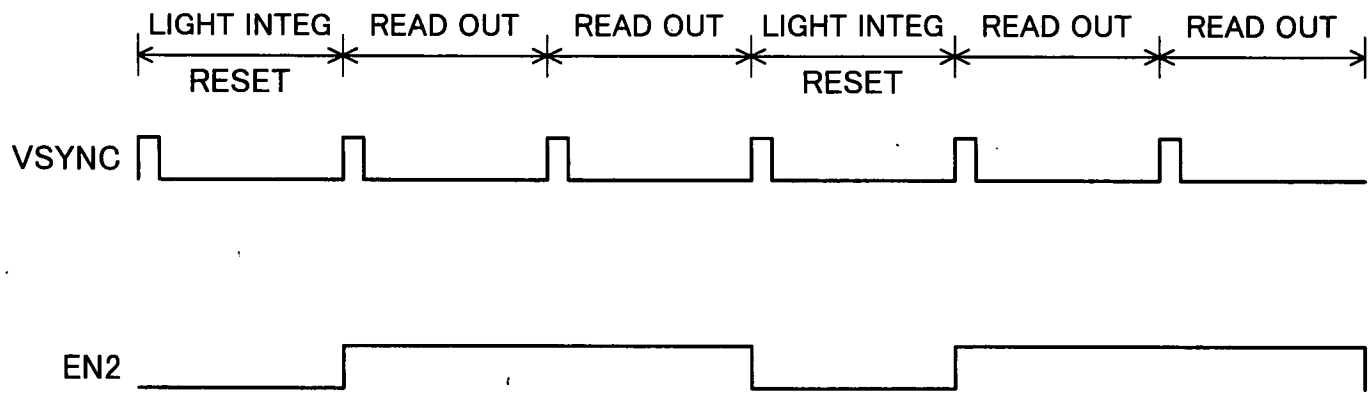

FIG.17

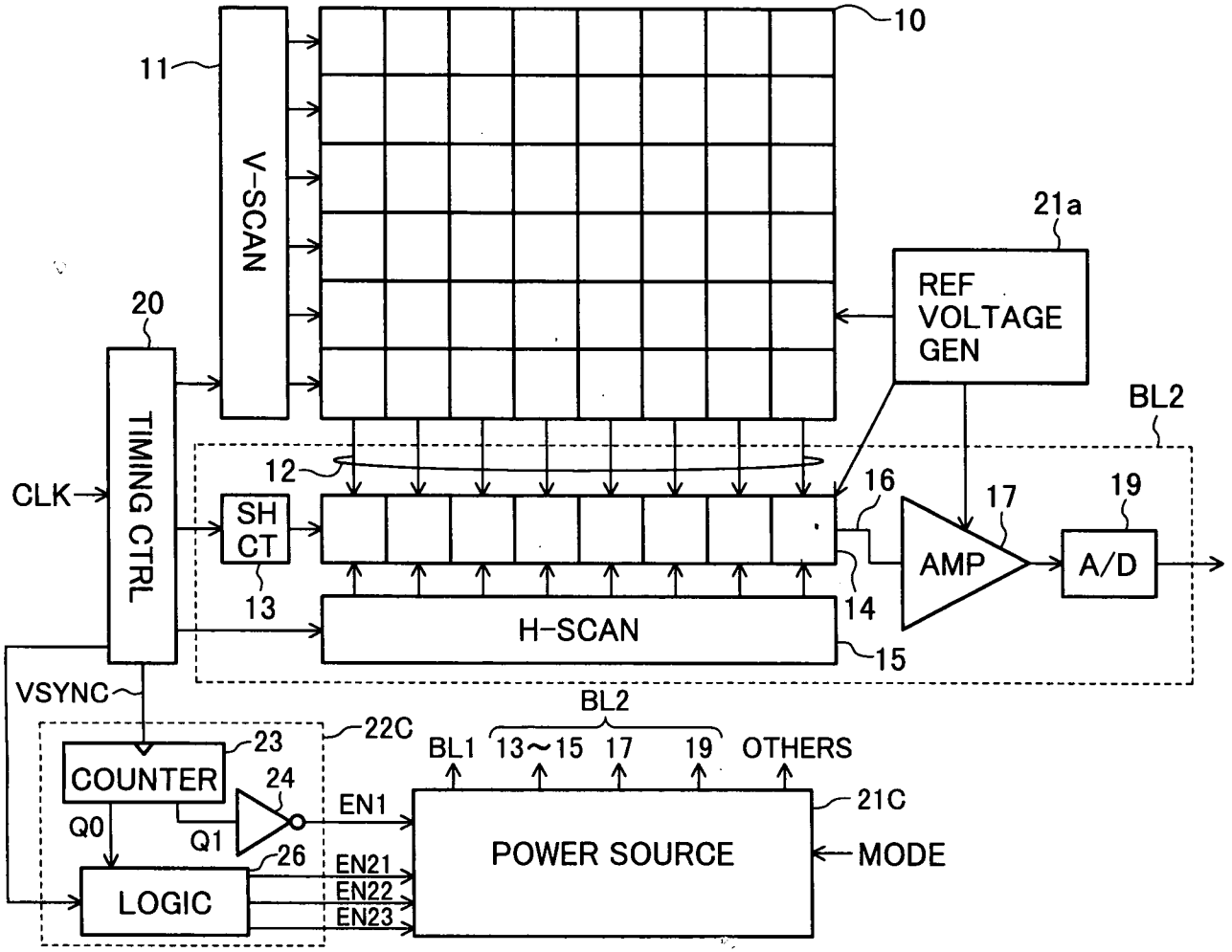
10
11
V-SCAN
21a
REF VOLTAGE GEN
20
TIMING CTRL
CLK
BL2
12
SH CT
13
16
17
19
AMP
A/D
14
H-SCAN
15
VSYNC
22C
BL2
BL1
13~15
17
19
OTHERS
23
COUNTER
24
EN1
21C
Q0
Q1
26
EN21
POWER SOURCE
MODE
LOGIC
EN22
EN23

FIG.18

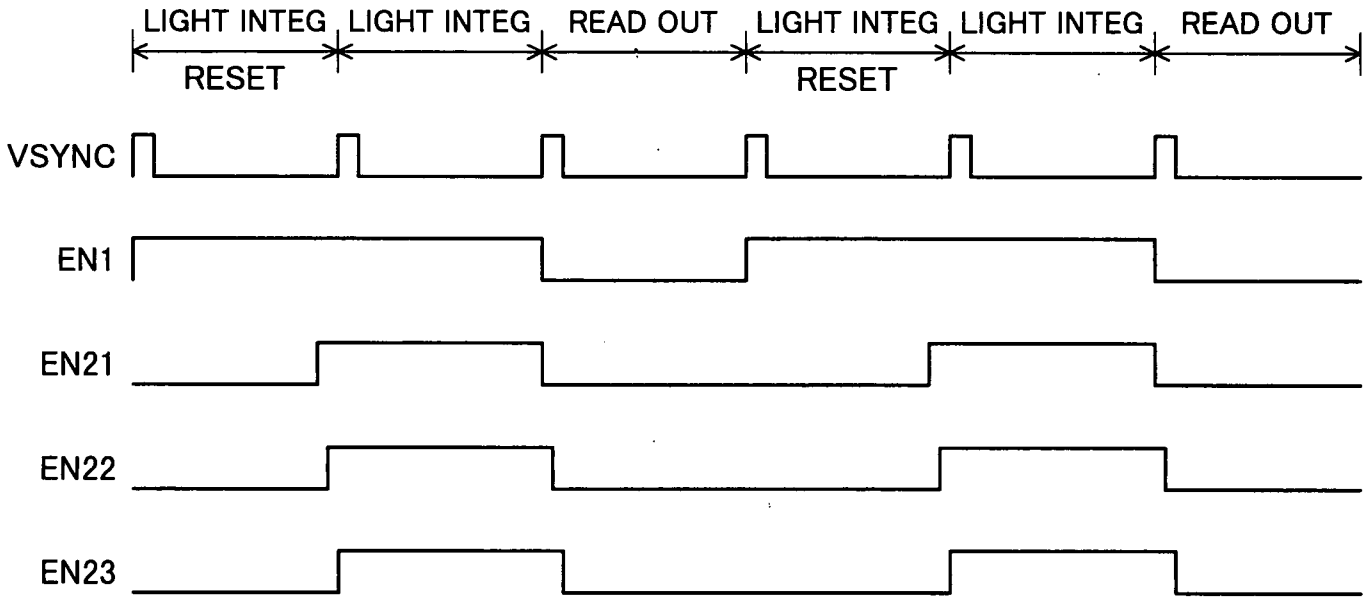

FIG.19
prior art